Please amend the following paragraphs in the specification:

Page 29, line 20, to page 30, line 4:

The synapse <u>circuits, S_1 to S_k, such as synapse</u> circuit S_1 202<u>, come</u> ~~comes~~ in two types. One type is adapted for interlayer connection, which is the connection between a neuron on the feature detection layer 102 and a neuron on the feature integration layer 103, and each layer may have connection with its subsequent layer or preceding layer. The other type is adapted for connection between neurons in the same layer. The latter type is used, as necessary, for connection between a pacemaker neuron, which will be discussed hereinafter, and a feature detection or integration neuron.

Page 31, lines 3 to 12:

The feature position detection layers 107 in the Where pathway shown in Fig. 1 receive the outputs of the feature <u>integration</u> ~~detection~~ layers 103 or the like of the What pathway. At lattice points that have been coarsely sampled while maintaining a positional relationship on the data input layer 101, only those neurons that are associated with the components useful for recognition (i.e., the components that have been registered beforehand from a pattern of a recognition category) in a feature extraction result on the What pathway will respond by means of filtering or the like.

Page 21, line 23, to page 33, line 12:

As another output mode of the Where pathway, an attended region of a predetermined size may be set on a data input layer from the feature salience map obtained from the output results of a feature detection layer 102 (1,0), and the position and size of the set region and the presence of the category of the object to be recognized therein may be output. As still another mode, a neural network may be applied wherein the receptive field hierarchically grows larger toward an upper layer, and in the uppermost layer, only the neuron that outputs a maximum value fires among the neurons associated with the category of a detected object. In such a system, the information regarding the dispositional relation or a spatial arrangement in a data input layer is stored to a certain extent also in the uppermost layer and intermediate layers.

Page 39, lines 14 to 25:

In the feature detection layer 102 (1,0), when it is assumed that there is a neuron N1 for detecting a structure (low-order feature) of a pattern that has a predetermined spatial frequency in a local region of a certain size and a predetermined directional component, if a corresponding structure exists in the receptive field of the neuron N1 on the data input layer 101, then the neuron N1 outputs a pulse in the phase based on the salience or contrast thereof. Such a function can be implemented by a Gabor filter. The following will describe a feature detection filtering function implemented by each neuron of the feature detection layer 102 (1,0).

Page 50, lines 6 to 15:

Fig. 4 shows the configuration of a synapse circuit S_i. Fig. 4A illustrates small synapse circuits 401 arranged in a matrix pattern to impart synaptic connection strength or phase delay to each neuron n'_j to which the neuron n_i is connected in a synapse circuit 202 (S_i). This arrangement allows the wiring from the synapse circuit to a target neuron to be accomplished on the same line, namely, a local common bus 301. In other words, the wiring between neurons can be virtually accomplished, thus improving or solving the wiring problem in prior arts.

Page 53, lines 6 to 15:

In this case, each small circuit shown in Fig. 4A can be a single circuit $S_{k,l}$ connected by the local common bus line 301 [[401]], as shown in Fig. 4B, thus achieving an especially economical circuit configuration. If the connection from the feature integration layer 103 or the sensor input layer 101 to the feature detection layer 102 is realized as described above, then the feature detection neurons detect an event in which a plurality of pulses representing different feature elements simultaneously arrive or substantially arrive at the same time.

Page 54, lines 1 to 14:

An example of the learning circuit at a synapse for implementing the simultaneous arrival of pulses or a predetermined phase modulation amount may include the circuit elements as shown in Fig. 5C. More specifically, the learning circuit 402 may be composed of a pulse propagation time measuring circuit 510, a time window generating

circuit 511, and a pulse phase modulation [[amount]] adjusting circuit 512 for adjusting the

pulse phase modulation amount at a synapse so as to set the propagation time at a

predetermined value. The propagation time in this case refers to the difference between the

time when a pulse was output at a preceding synapse of a neuron of a certain layer and the

time when the pulse arrives at a destination neuron of the succeeding layer.

Page 69, line 18, to page 70, line 10:

Fig. 8 is a flowchart illustrating the processing procedure of each layer

described above. The flowchart summarizes the flow of the processing from the detection

of low-order features to the detection of high-order features. First, in step S801, a layer

performs the detection of low-order features, including the calculation of a Gabor wavelet

transform coefficient at each position. Then, in step S802, the layer performs the

integration processing of the low-order features, such as local averaging of the features.

The layer detects and integrates medium-order features in steps S803 and S804,

respectively, then detects and integrates high-order features in steps S805 and S806,

respectively. In step S807, an output regarding whether an object to be recognized or

detected is present, or an output regarding the detected position of the object is supplied as

the output of the final layer. The number of layers assigned to steps S803 and S804, and

S805 and S806 can be arbitrarily set or changed according to a subject, such as an object to

be recognized.

Page 71, lines 4 to 18:

The procedure of the processing implemented by each feature integration neuron is as shown by the flowchart of Fig. 10. In step S1001, the feature integration neuron receives a pulse input from a feature detection neuron that provides a detection processing module 104 for detecting features of the same category and provides a local receptive field intrinsic to the neuron. In step S1002, the feature integration neuron adds input pulses for a predetermined time width, which means a time range other than a refractory period. In step S1003, the feature detection neuron determines whether the total sum value of the input pulses, which may be measured, for example, on the basis of a potential, has reached a threshold value, and if the determination result is affirmative, then the neuron outputs a pulse in a phase based on the total sum value.

Page 77, lines 11 to 17:

Fig. 12A shows a configuration unit of a small synapse circuit element 401 used in this embodiment. A learning circuit 402 of the same kind of the one in the first embodiment and a pulse width modulating circuit 1201 are included. For the pulse width modulating circuit 1201, a well-known circuit, such as the one disclosed in the gazette of Patent No. 2717662 by the present assignee, may be used.

Page 77, line 18, to page 78, line3:

Instead of performing the aforesaid pulse width modulation, a pulse frequency may be modulated at each synapse element. In this case, the configuration of the small synapse circuit element 401 that corresponds to the above configuration includes the

learning circuit 402 and a pulse frequency modulating circuit 1202, as shown in Fig. 12B.

A known configuration may be applied to the pulse frequency modulating circuit 1202.

The modulation by the synapse is expressed by $f_a=S_{ij}f_b$ when the pre-synaptic pulse

frequency is denoted as f_b, and the post-synaptic pulse frequency is denoted as f_a

Page 83, lines 3 to 9:

In this embodiment, the feature detection layers 102 (1,0), (1,1), and feature

integration layers 103 (2,0), (2,1), shown in Fig. 1 form a set of processing channels at a

plurality of resolutions or scale levels as a whole. Each processing channel implements

processing at one scale level or resolution to detect and recognize low- to high-order

features by hierarchical parallel processing.

Page 89, line 21, to page 90, line 10:

The mechanism of the population coding performed by the latter type of

neurons will be explained in detail. The population coding neurons perform integration by

performing normalized linear coupling of the outputs from a plurality of sub-sampling

neurons that are at the same hierarchical level (i.e., the complexity of a graphic feature is at

about the same level), but belong to different processing channels for the same feature, and

exist in the same feature integration layer. For example, the feature integration layer 103

(2,0) that receives the outputs of the feature detection layer 102 (1,0) carrying out Gabor

wavelet transform integrate, by linear combination or the like, the outputs associated with a

set $\{g_{mn}\}$ (n is constant, and m=1,2,...) of Gabor filters that belong to different processing

channels, but have the same directional selectivity.

Page 99, lines 13 to 20:

The sum of squares calculating circuit 1703 has an inter-neuron circuit 1706

for pooling the square values of feature detection cells, and a ~~synapse~~ synaptic connection

~~element~~ 1702 for applying a connection to the inter-neuron circuit 1706 imparts a pulse

phase delay, a pulse width modulation, or a pulse frequency modulation equivalent to the

square value of an output of the feature detection neuron element 1701.

Page 101, lines 8 to 18:

For the WTA circuit, a known configuration may be employed, such as the

one disclosed in Japanese Patent Laid-Open No. 08-321747, USP5059814, or

USP5146106. Fig. 19A schematically shows the configuration wherein the outputs of only

the processing channels indicating maximum responses in a feature integration layer are

propagated by the WTA circuit to a feature detection layer (the succeeding layer) in the

feature integration layer. This circuit configuration is identical to the one shown in Fig. 18

except that the channel activation degree control circuit 1802 of Fig. 18 has been replaced

by a gating circuit 1902.

Page 101, lines 19 to 24:

As shown in Fig. 19B, the gating circuit 1902 has a WTA circuit 1903

[[1603]] that receives a mean output level for each processing channel, and a channel

selecting circuit 1904 [[1604]] for propagating the output of each neuron from a processing

channel indicating a maximum mean output level to the same channel of the next layer.

Page 111, line 16, to page 112, line 2:

Fig. 23 shows the transition of signal trains. In order to obtain scale-invariant representation of information by pulse phase modulation, phase conversion is carried out once by a pulse phase converter 2101 shown in Fig. 21 so that pulses of different processing channels are placed at different positions on a time base and that pulse signals belonging to different processing channels are not mixed (see Fig. 23A). Then, scale-invariant pulse signal trains are obtained by a scale-invariant signal converter 2102, and the pulse trains from the feature integration layer 103 (2,0) are caused to arrive at the neurons of the feature detection layer 102 (1,1).

Page 117, line 25, to page 118, line 13:

As in the case of the fifth embodiment, multi-scale processing can be implemented by a single circuit in the layers from the feature detection layer 102 (1,1) and after, without the need for providing a different circuit for each processing channel, thus permitting economical circuit configuration to be attained. In other words, as shown in Fig. 22, the physical discrimination among different processing channels can be eliminated in circuit configuration from the layer (1,1) and after. In this embodiment, the coupling and population coding corresponding to expressions (9) and (10), respectively, are performed in the time domain on the signals of the scale levels or processing channels disposed at temporally different positions, in the layer (1,1) and after.

Page 118, lines 14 to 24:

The outputs from the feature detection layer 102 (1,1) to a feature integration layer 103 (2,1) are supplied in a time sharing mode for each processing channel or scale level. This applied to all the succeeding layers. More specifically, when performing temporal integration on input signals of feature detection cells, pulses for one processing channel are output in correspondence to the entire range of a sub time window making up one scale level. The population coding in the feature integration layer is implemented by integrating input pulses in the time windows involving multiple channels.

Page 124, line 23, to page 125, line 17:

Feature detection layers (1,k) form, as a whole, processing channels of a plurality of resolutions or scale levels. Specifically, taking an example wherein the Gabor wavelet transform is performed by a feature detection layer 102 (1,0), a set of feature detection cells having Gabor filter kernels in their receptive field structures that share the same scale level but have different directional selectivities belongs to the same procesing channel in the feature detection layer 102 (1,0), as shown in Fig. 12. In the succeeding layer (1,1), the feature detection cells for detecting higher-order features that receive the outputs from the feature detection cells belong to the same processing channel. In further succeeding layers (1,k), in which k>1, the feature detection cells that receive the outputs from a plurality of feature integration cells that form the same channel in a layer (2,k-1) belong to that channel also. In each processing channel, processing at the same scale level or resolution is implemented to detect and recognize low-order features to high-order features through the hierarchical parallel processing.

- 10 -

Page 125, line 18, to page 126, line 5:

The feature integration layer 103 (2,0) on the What pathway has a predetermined receptive field structure and is composed of neuron elements that generate pulse trains. Hereinafter, the receptive field will mean the range of connection to the output elements of an immediately preceding layer, and the receptive field structure will mean the distribution of the connection weights. The neuron feature integration layers U103U (2,0) integrate a plurality of neuron element outputs in the receptive fields from the feature detection layer U102U (1,0). The integration is carried out by sub-sampling by local averaging or the like, and by computation, such as coupling of the results of processing at different scale levels.

Page 126, lines 6 to 16:

Each receptive field of the neurons in the feature integration layer share the same structure as long as the neurons belong to the same layer. Feature detection layers 102 ((1,1) (1,1), (1,2), ..., (1,N)) and feature integration layers 103 ((2,1), (2,2), ..., (2,N)) have predetermined receptive field structures individually acquired by learning. As in the case of the aforesaid layers, the former layers ((1,1), ...) detect a plurality of different features in individual feature detection modules, and the latter layers ((2,1), ...) integrate detection results regarding a plurality of features received form a preceding feature detection layer.

- 11 -

Page 135, line 21, to page 136, line 14:

Figs. 31 and 32 show the examples of the pathways of signal propagation among the fixation region setting control layer 108, a feature integration layer (2,0) and a feature detection layer (1,1). The configurations shown in both Figs. 31 and 32 employ a gating circuit 3101 that is provided together with a common bus of a digital circuit and has a switching function, and a switching signal control circuit 3102 for controlling the ON/OFF of the switching function at high speed. Referring to Fig. 31, the <u>attention fixation</u> control neuron 2901 makes a connection to a neuron in a region of a predetermined size unique to the processing channel of a neuron that belongs to a region 109 centering about a plurality of neurons of the feature integration layer (2,0), i.e., the neurons on the feature integration layer that are associated with fixation positions (hereinafter referred to as "attention-center neurons"). The size of the region 109 is intrinsic to the processing channel to which the attention-center neurons on an integration layer belong.

Page 139, line 24, to page 140, line 11:

In this case, the input distribution control circuit 3302 connects to the synapse <u>circuit</u> 3301 involved in the modulation of the detection level of the salience map signal inputs of low-order features received from lower layers, and also to another synapse <u>circuit</u> 3301 involved in the modulation of the detection level of feedback signals from upper layers. The input distribution control circuit 3302 mainly controls the phase delay amounts at the synapses corresponding to the values of h_1 and h_2 in response to external control signals (e.g., a signal regarding a subject received from a further upper layer, not

shown in Fig. 1, the signal indicating whether a particular mode is the one for detecting an object or for detailed identification).

Page 144, lines 10 to 16:

After a next candidate fixation position is selected, the secondary feedback signal amplifier 3006 [[1906]] amplifies a feedback signal from an upper layer to an attention control neuron to a predetermined level by means of advancing a pulse phase in the case of phase modulation, then the amplified feedback signal is returned to the attention control neuron.

Page 149, line 25, to page 150, line 14:

In step S3707, as the result of the updating, the attention control neuron receiving a quasi-maximum semi-maximum feedback amount mentioned above is activated, and a signal for setting the next fixation region is output from the activated neuron to a feature integration layer in the case shown in Fig. 31 or to a gating layer in the case shown in Fig. 32. In step S3708, a part of a particular processing channel is opened thereby to propagate the signal from the feature integration layer neuron associated with the updated fixation region to a feature detection layer (1,1). On the other hand, if it is decided not to perform updating as a result of determining whether the attention should be updated (refer to the three cases of determinations described above), then the control operation for updating the fixation region is terminated.

Page 165, lines 9 to 19:

In the tenth embodiment, as shown in Fig. 39, a subject detecting or recognizing apparatus 1111 is installed in an image input apparatus, such as a camera or a video camera. The apparatus 1111 includes an assisting information detector 3902 for detecting information, such as the position and the size of an object, an image of which is intended to be input or photographed by a user or a photographer, and a fixation region setting controller 3901 according to the embodiments described above. In this embodiment, the assisting information detector 3902 will be described, taking a visual axis as an example.

Page 165, line 20, to page 166, line 5:

The assisting information detector or the visual axis detector 3902 and the fixation region setting controller 3901 work together to carry out the control for setting a fixation position. This arrangement makes it possible to achieve automatic high-speed photographing that is ideally suited to a particular object in the image and that enables user's intention to be reflected. The assisting information in addition to the visual axis may be explicitly set by a user. In the following description, the assisting information detector 3902 will be called as "the visual axis detector 3902".

Page 167, lines 3 to 7:

The visual axis detector <u>3902</u> [[3901]] may employ the configuration

disclosed in Patent No. 2505854, Patent No. 2763296, or Patent No. 2941847 by the

assignee, or another similar configuration. The description of the configuration, therefore,

will be omitted.